

# **AD145A4 Datasheet**

**Zhuhai Jieli Technology Co.,LTD**

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# AD145A4 Features

## CPU Core

- 32-bit CPU, the highest frequency is 160MHz
- Maximum 16KB 4Way ICache, configurable part Way as a common memory for the CPU use or other Peripheral

## Memory

- On-chip 32KB SRAM(not including ICache)
- ICache SRAM: 4KB~12KB configurable

## Clock Source

- RC Clock frequency about 16MHz
- LRC( low power RC) clock frequency about 32KHz
- HTC( low drift internal high frequency RC)clock frequency is 5MHz

## Digital I/O

- 16 programmable digital I/O pins
- USB DP/DM can be configured to normal I/O pins
- General the IO supports pull-up(10k),pull-down(60k), strong,weak output,input and high impedance
- Up to 8 external interrupt/wake-up source(low power available,can be multiplexed to any I/O, with hardware filter)
- Input channel and Output channel, provide arbitrary IO input and output options for some modules

## Digital peripherals

- One Full Speed USB 1.1 PHY

- Two UART Controllers(UART0/1)  
UART1 supports DMA and Flow Control
- Two SPI Controllers with DMA(SPI0/1)  
support master mode and slave mode.
- One Spi Flash Controller to run code
- Built-in SPI flash
- I2S audio interface
- Two 16-bit Asynchronous Divider Timers
- One IIC Controller
- Four channel PWM output
- 0.5 watt Class-D audio amplifier output
- Infrared remote control decoder
- Watchdog
- 64-bit EFUSE

## Analog Peripherals

- MIC amplifier circuit
- Two analog audio input channels
- 10-bit high precision ADC
- 16-bit high precision ADC (mainly as recording)
- 16-bit high precision DAC
- Low voltage protection
- Power on reset

## Operating Conditions

- Working voltage  
VBAT: 2.0v - 5.5v  
VDDIO: 2.0v - 3.4v
- Operating Temperature: -40°C to +85°C

## Package

- QSOP24

## Application

- Sound Toy
- Audio player

# 1、 Pin Definition

## 1.1 Pin Assignment

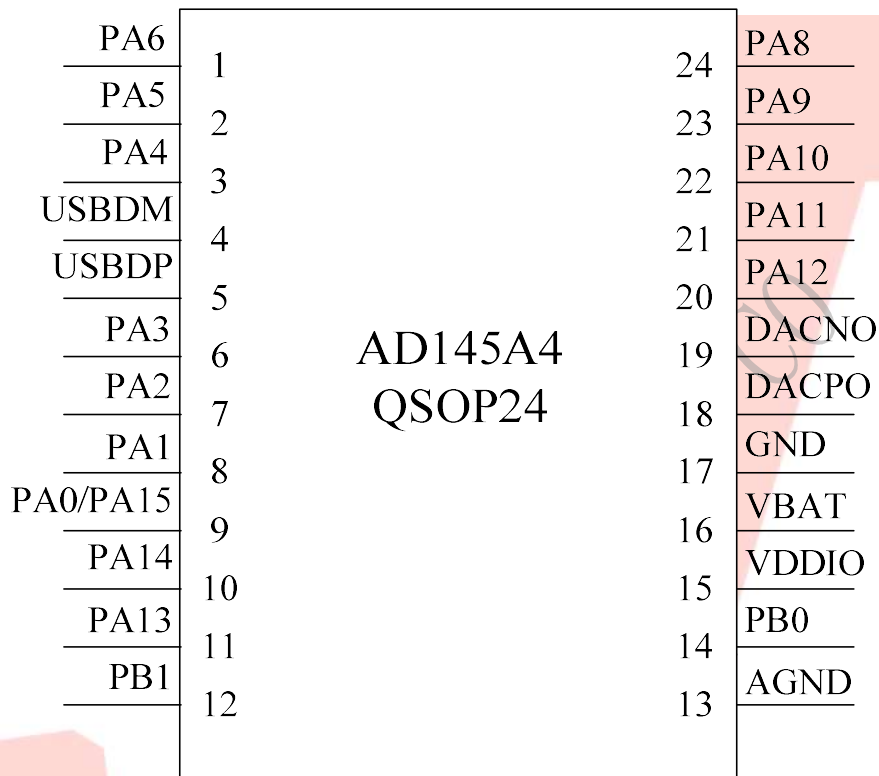


Figure 1-1 AD145A4\_QSOP24 Package Diagram

## 1.2 Pin Description

Table 1-1 AD145A4\_QSOP24 Pin Description

PIN NO.	Name	Type	Drive (mA)	Function	Description
1	PA6	I/O	8/64	GPIO	I2S_MCLK:Audio Link Master Clock; SPI1DIC:SPI1 Data In(C); SD0DATD:SD0 Data(D);
2	PA5	I/O	8/64	GPIO	ADC7:ADC Input Channel 7; SPI0DAT3:SPI0 Data Out3 SPI1DOC:SPI1 Data Out(C); SD0CMDC:SD0 Command(C); SD0CMD:SD0 Command(D); UART0RXA:Uart0 Data In(A); I2C_SDA(C); PWM1:PWM Channel1 Output;
3	PA4	I/O	8/64	GPIO	ADC6:ADC Input Channel 6; SPI0DAT2:SPI0 Data 2; SPI1CLKC:SPI1 Clock(C); SD0CLKC:SD0 Clock(C); SD0CLKD:SD0 Clock(D); UART0TXA:Uart0 Data Out(A); I2C_SCL(C); TMR2:Timer2 Clock In; PWM0:PWM Channel0 Output;
4	USBDM	I/O	10	USB Negative Data (pull down)	ADC5:ADC Input Channel 5; SPI1DOA:SPI1 Data Out(A); SD0DATC:SD0 Data(C); UART1TXA:Uart1 Data Out(A); I2C_SDA(A);
5	USBDP	I/O	10	USB Positive Data (pull down)	ADC4:ADC Input Channel 4; SPI1CLKA:SPI1 Clock(A); UART1RXA:Uart1 Data In(A); I2C_SCL(A);
6	PA3	I/O	8/64	GPIO	ADC3:ADC Input Channel 3; SPI0DIB(1):SPI0 Data1 In(B); SPI1DIA:SPI1 Data In(A); SD0DATA:SD0 Data(A); PWM2L; MCAP0:Motor Timer0 Capture;

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7	PA2	I/O	8/64	GPIO	ADC2:ADC Input Channel 2; SPI0DOB(0):SPI0 Data0 Out(B); SD0CMDA:SD0 Command(A); I2C_SDA(B); PWM2H;
8	PA1	I/O	8/64	GPIO	ADC1:ADC Input Channel 1; SPI0CLKB:SPI0 Clock(B); SD0CLKA:SD0 Clock(A); UART0RXB:Uart0 Data In(B); I2C_SCL(B); CAP2:Timer2 Capture;
9	PA0	I/O	8/64	GPIO (pull up)	Long Press Reset; ADC0:ADC Input Channel 0; UART0TXB:Uart0 Data Out(B);
	PA15	I/O	8/64	GPIO	ADC12:ADC Input Channel 12; MIC_LDO:Microphone Power Output;
10	PA14	I/O	8/64	GPIO	ADC11:ADC Input Channel 11; AUX1:Analog Channel 1 Input;
11	PA13	I/O	8/64	GPIO	ADC10:ADC Input Channel 10; AUX0:Analog Channel 0 Input; MIC_BIAS:Microphone Bias Output; CAP0:Timer0 Capture
12	PB1	I/O	8/64	GPIO	MIC_IN: MIC Input Channel;
13	AGND	G	/		Analog Ground;
14	PB0	I/O	8/64	GPIO	<b>DAC:Analog Audio Output;</b> ADC13:ADC Input Channel 13; LVD:Low Voltage Detect;
15	VDDIO	P	/		GPIO Power;
16	VBAT	P	/		Battery Power Supply;
17	GND	G	/		Digital Ground;
18	DACPO	O	/		Class-D APA Positive Output;
19	DACNO	O	/		Class-D APA Negative Output;
20	PA12	I/O	8/64	GPIO	I2S_LRCK:Audio Link Word Select; SPI1DOB:SPI1 Data Out(B); SD0CMDB:SD0 Command(B); MCAP3:Motor Timer3 Capture;
21	PA11	I/O	8/64	GPIO	ADC9:ADC Input Channel 9; I2S_SCLK:Audio Link Serial Clock; SPI1CLKB:SPI1 Clock(B); SD0CLKB:SD0 Clock(B); MCAP2:Motor Timer2 Capture;

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22	PA10	I/O	8/64	GPIO	ADC8:ADC Input Channel 8; I2S_DAT3:Audio Link Data3; SPI1DIB:SPI1 Data In(B); SD0DATB:SD0 Data(B); TMR1:Timer1 Clock In; MCAP1:Motor Timer1 Capture;
23	PA9	I/O	8	GPIO (High Voltage Resistance)	I2S_DAT2:Audio Link Data2; UART1TXB:Uart1 Data Out(B); UART1RXB:Uart1 Data In(B); I2C_SDA(D); CAP1:Timer1 Capture; PWM3:PWM Channel3 Output;
24	PA8	I/O	8	GPIO (High Voltage Resistance)	I2S_DAT1:Audio Link Data 1; I2C_SCL(D); TMR0:Timer0 Clock In; PWM2:PWM Channel2 Output; OSCI:Crystal Oscillator Input;

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## 2、Electrical Characteristics

### 2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Tamb	Ambient Temperature	-40	+85	°C
Tstg	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	-0.3	5.5	V
V <sub>VDDIO33</sub>	3.3V IO Input Voltage	-0.3	3.6	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

### 2.2 PMU Characteristics

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.0	3.7	5.5	V	—
V <sub>VDDIO</sub>	Voltage output	2.0	3.0	3.4	V	VBAT = 3.7V, 100mA loading
I <sub>VDDIO</sub>	Loading current	—	—	100	mA	VBAT=3.7V

### 2.3 IO Input/Output Electrical Logical Characteristics

Table 2-3

IO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V <sub>IL</sub>	Low-Level Input Voltage	-0.3	—	0.3* VDDIO	V	VDDIO = 3.3V
V <sub>IH</sub>	High-Level Input Voltage	0.7* VDDIO	—	VDDIO+0.3	V	VDDIO = 3.3V
IO output characteristics						
V <sub>OL</sub>	Low-Level Output Voltage	—	—	0.33	V	VDDIO = 3.3V
V <sub>OH</sub>	High-Level Output Voltage	2.7	—	—	V	VDDIO = 3.3V

## 2.4 Internal Resistor Characteristics

Table 2-4

Port	General Output	High Drive	Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA0~PA6、 PA10~PA15、 PB0、PB1	8mA	64mA	10K	60K	1、PA0 default pull up 2、USBDM & USBDP default pull down 3、internal pull-up/pull-down resistance accuracy $\pm 20\%$
PA8、PA9 (high voltage I/O)	8mA	–	10K	60K	
USB DP	10mA	–	1.5K	15K	
USB DM	10mA	–	180K	15K	

## 2.5 Analog DAC(PB0) Characteristics

Table 2-5

Parameter	Min	Typ	Max	Unit	Test Conditions
Frequency Response	20	–	16K	Hz	1KHz/0dB 100kohm loading With A-Weighted Filter
THD+N	–	-65	–	dB	
S/N	–	95	–	dB	
Output Swing	–	0.54	–	Vrms	
Dynamic Range	–	92	–	dB	1KHz/-60dB 100kohm loading With A-Weighted Filter
Output Resistance	–	8.3	–	K	–

## 2.6 ADC Characteristics

Table 2-6

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range	–	75	–	dB	1KHz/210mVrms line mode :6dB with cap PGAIS=2
S/N	–	79	–	dB	
THD+N	–	-70	–	dB	

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### 3、 Package Information

#### 3.1 QSOP24

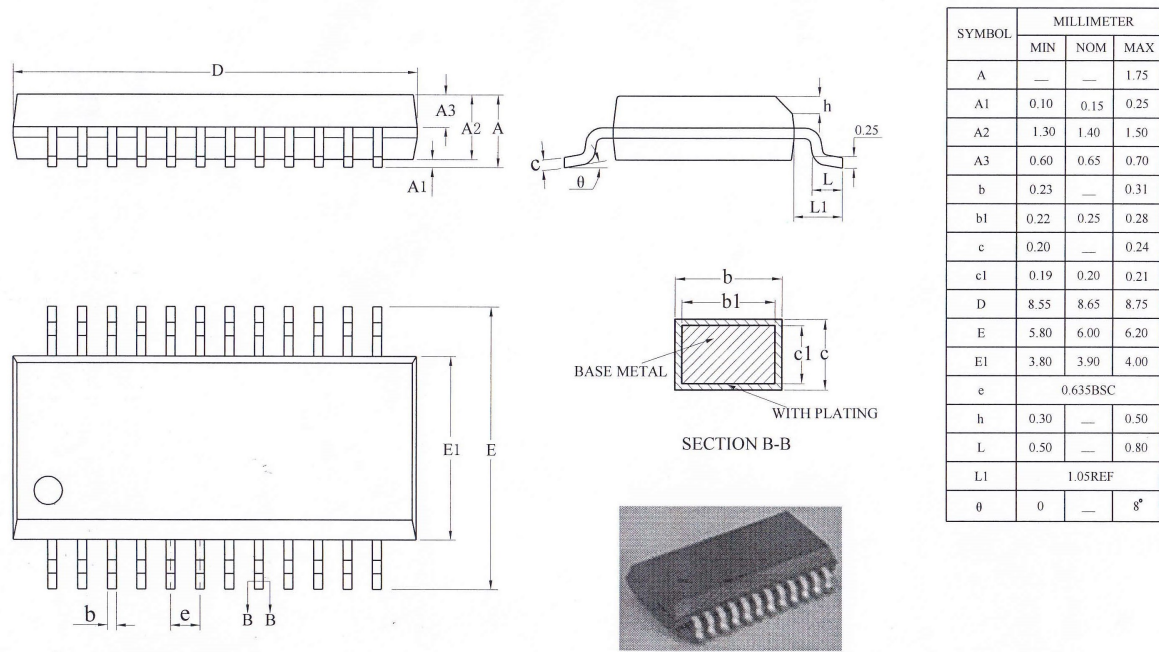


Figure 3-1. AD145A4\_QSOP24 Package

## 4、 Revision History

Date	Revision	Description
2021.03.09	V1.0	Initial Release

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